

# MC100LVELT20

## 3.3 V LVTTTL/LVCMOS to Differential LVPECL Translator

### Description

The MC100LVELT20 is a 3.3 V TTL/CMOS to differential PECL translator. Because PECL (Positive ECL) levels are used, only + 3.3 V and ground are required. The small outline SOIC-8 package and the single gate of the MC100LVELT20 makes it ideal for those applications where space, performance, and low power are at a premium.

The 100 Series contains temperature compensation.

### Features

- 390 ps Typical Propagation Delay
- Maximum Input Clock Frequency > 0.8 GHz Typical
- Operating Range  $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$  with  $GND = 0\text{ V}$
- PNP TTL Input for Minimal Loading
- Q Output will Default HIGH with Input Open
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



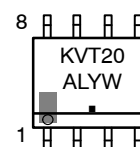
ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)



SOIC-8 NB  
D SUFFIX  
CASE 751-07

### MARKING DIAGRAM



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

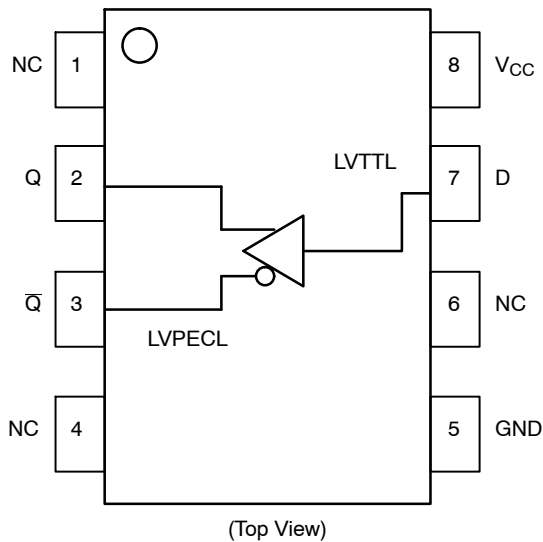
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

Device	Package	Shipping†
MC100LVELT20DG	SOIC-8 NB (Pb-Free)	98 Units/Tube
MC100LVELT20DR2G	SOIC-8 NB (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MC100LVELT20



**Table 1. PIN DESCRIPTION**

Pin	Function
Q, $\bar{Q}$	Differential PECL Outputs
D	LVTTTL Input
V <sub>CC</sub>	Positive Supply
GND	Ground
NC	No Connect

**Figure 1. 8-Lead Pinout and Logic Diagram**

**Table 2. ATTRIBUTES**

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 1.5 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
SOIC-8 NB	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	150 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Power Supply	GND = 0 V		6	V
V <sub>I</sub>	Input Voltage	GND = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	6	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 NB	190 130	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8 NB	41 to 44	°C/W
T <sub>sol</sub>	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## MC100LVELT20

**Table 4. LVTTTL INPUT DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{IH}$	Input HIGH Current ( $V_{in} = 2.7\text{ V}$ )			20	$\mu\text{A}$
$I_{IHH}$	Input HIGH Current MAX ( $V_{in} = 6.0\text{ V}$ )			100	$\mu\text{A}$
$I_{IL}$	Input LOW Current ( $V_{in} = 0.5\text{ V}$ )			-0.6	$\text{mA}$
$V_{IK}$	Input Clamp Voltage ( $I_{in} = -18\text{ mA}$ )			-1.2	$\text{V}$
$V_{IH}$	Input HIGH Voltage	2.0			$\text{V}$
$V_{IL}$	Input LOW Voltage			0.8	$\text{V}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**Table 5. 100LVELT PECL OUTPUT DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ,  $GND = 0\text{ V}$  (Note 1))

Symbol	Characteristic	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{CC}$	Negative Power Supply Current	20	25	30	22	27	32	23	28	33	$\text{mA}$
$V_{OH}$	Output HIGH Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	$\text{mV}$
$V_{OL}$	Output LOW Voltage (Note 2)	1355	1480	1605	1355	1480	1605	1355	1480	1605	$\text{mV}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Output parameters vary 1:1 with  $V_{CC}$ .
- All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

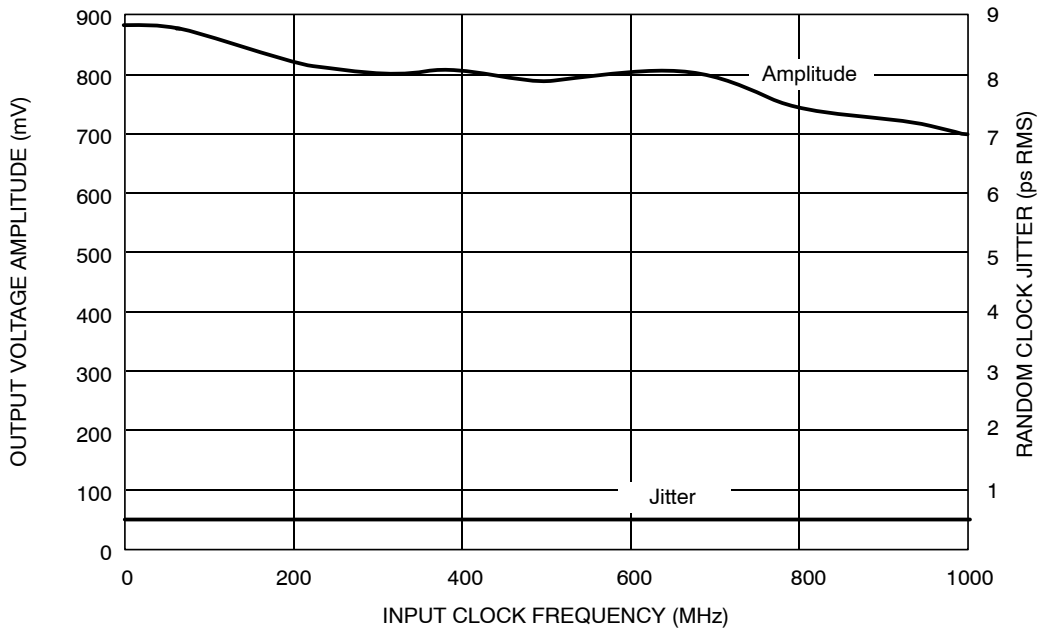
**Table 6. AC CHARACTERISTICS** ( $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $GND = 0\text{ V}$  (Note 1))

Symbol	Characteristic	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{max}}$	Maximum Input Clock Frequency (Figure 2)	600	800		600	800		600	800		$\text{MHz}$
$t_{\text{PLH}}$ , $t_{\text{PHL}}$	Propagation Delay to Output Differential	280	350	430	300	370	450	320	400	490	$\text{ps}$
$t_{\text{SKEW}}$	Device-to-Device Skew (Note 2)			250			250			250	$\text{ps}$
$t_{\text{JITTER}}$	Random Clock Jitter (RMS) (Figure 2)		< 1	< 2		< 1	< 2		< 1	< 2	$\text{ps}$
$t_r$ , $t_f$	Output Rise/Fall Times Q, $\bar{Q}$ (20% – 80%)	70	100	225	80	120	225	90	140	225	$\text{ps}$

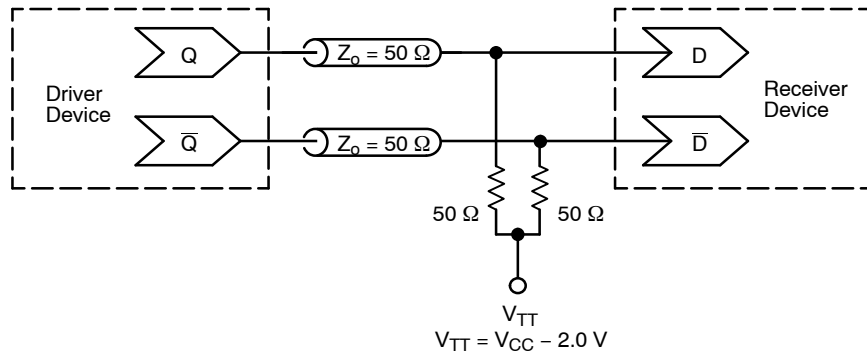
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Measured using a LVTTTL source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .
- Skew is measured between outputs under identical transitions.

# MC100LVELT20



**Figure 2. Output Voltage Amplitude ( $V_{OUTpp}$ )/RMS Jitter vs. Input Clock Frequency at Ambient Temperature**



**Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)**

## MC100LVELT20

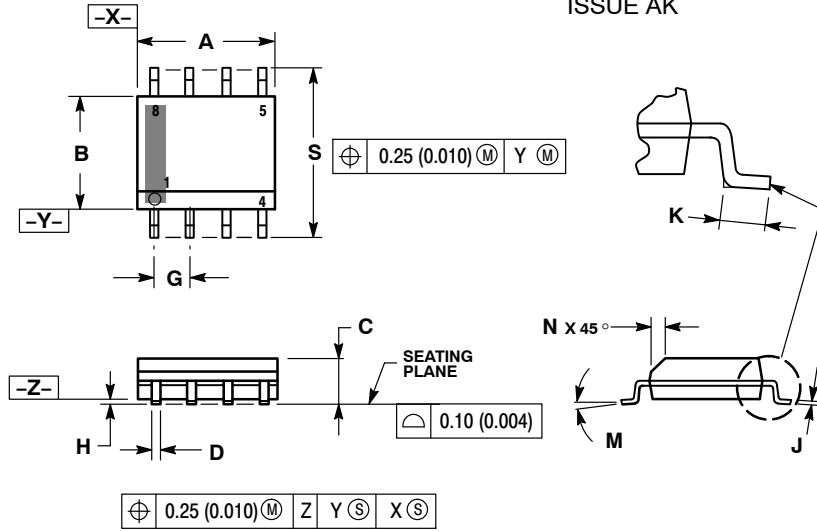
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC100LVELT20

## PACKAGE DIMENSIONS

### SOIC-8 NB CASE 751-07 ISSUE AK

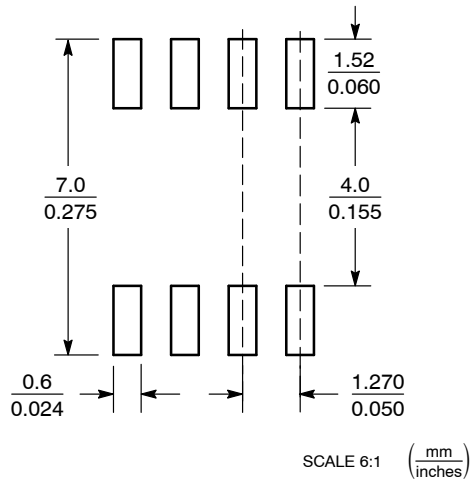


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDERRM/D](#).\*

ECLinPS is a registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative